

## **CE-ATA Technical Errata**

Errata ID	Protocol 020
Affected Spec Ver.	Protocol 1.0
Corrected Spec Ver.	

## Submission info

Name	Company	Date
Amber Huffman	Intel	12/20/2005

Description of the specification technical flaw (add space as needed)

The MMC Command state machine does not indicate to the MMC Data state machine that MMC Busy may be asserted when a CMD12 is received. This erratum corrects that oversight.

# Description of the correction

# State DC16: DC\_Cmd12\_Entry in section 2.4.2.1.3 shall be modified as shown:

DC16:	: DC	_Cmd12_Entry	Device pulls up the CMD line. Notify A abort. Notify MMC Data layer to stop a MMC Busy may be asserted if a write it.	any da	ata transmission and that
	1.	R1 response is re	ady for transmission.	$\rightarrow$	DC_Cmd12_R1
	2.	R1 response is no	t ready for transmission.	$\rightarrow$	DC_Cmd12_Entry

# Disposition log

12/20/2005 Erratum captured 12/30/2005 Added that MMC Busy may only be asserted if a write is in progress 3/12/2005 Erratum ratified
--

Technical input submitted to the CE-ATA Workgroup is subject to the terms of the CE-ATA contributor's agreement.